INTERFACES FOR CATV / SMATV HEADENDS AND SIMILAR PROFESSIONAL EQUIPMENT

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Foreword

The revision of this specification was prepared by the DVB-TM ad hoc group on Physical Interfaces. The Technical Module of the DVB project approved the technical content of this specification which now constitutes the basis for a European standardization process for the application range described under "Scope".

1 Scope

This specification describes physical interfaces for the interconnection of signal processing devices for professional CATV/SMATV headend equipment or for similar systems, such as in uplink stations. Especially this document specifies the transfer of MPEG 2 data signals in the standardized transport layer format between devices of different signal processing functions.

RF interfaces and interfaces to telecom networks are not covered in this document:

- For RF interfaces reference is made to CENELEC publication EN 50083 (Cabled distribution systems for television and sound signals, part 5: Headend equipment) and amendments [1].
- For connections to telecom networks a special Data Communication Equipment (DCE) is necessary to adapt the serial or parallel interfaces specified in this document to the bitrates and transmission formats of the public Plesiochronic Digital Hierarchy (PDH) networks. Other emerging technologies such as Connectionless Broadband Data Services (CBDS), Synchronous Digital Hierarchy (SDH), Asynchronous Transfer Mode (ATM) etc. can be used for transmitting DVB/MPEG2 Transport Streams between remote locations. ATM is particularly suitable for providing bandwidth on demand and it allows for high data rates.

2 Normative references

2.1 ETSI Publications

ETS 300 158	Satellite Earth Stations (SES) Television Receive-Only (TVRO-FSS), Satellite Earth Stations operating in the 11/12 GHz FSS bands
ETS 300 249	Satellite Earth Stations (SES) Television Receive-Only (TVRO) equipment used in the Broadcasting Satellite Service (BSS)
ETS 300 473	Digital broadcasting systems for television, sound and data services, Satellite Master Antenna Television (SMATV) distribution systems.

2.2 Cenelec Publications

[1] Amendments to Cenelec EN50083 are expected shortly as a result from the DIGISMATV project.

EN 50083-5	Cabled distribution systems for television and sound signals, Part 5: Headend equipment

2.3 ITU Publications

CCIR Rec.G.656	Interfaces for digital component video signals in 525-line and 625-line television signals.
CCITT (ITU-T) Rec.G.651	Specifications of multimode fiber
CCITT (ITU-T) Rec.G.652	Specifications of single mode fiber
CCITT (ITU-T) Rec.G.703	General aspects of digital transmission systems - Terminal Equipment. Physical/electrical characteristics of hierarchical digital interfaces
CCITT (ITU-T) Rec.G.956, CCITT (ITU-T) Rec.G.957	Optical interfaces for equipments and systems relating to the synchronous digital hierarchy

2.4 ISO and IEC Publications

IEC 793-2	Optical fibres; part 2: product specifications
IEC 874-14	Connectors for optical fibres and cables, Part 14: Sectional specification for fibre optic connector, type SC.
ISO 2110 (1989)	Information technology, Data communication, 25 pole DTE/DCE interface connector and contact number assignments.
ISO 9314-3	Information processing systems; fibre distributed data interface (FDDI); part 3: physical layer medium dependent (PMD)
ISO 13818-1:	Information Technology - Generic coding of moving pictures and associated audio information - Part 1: Systems

2.5 Other Publications

EIA/TIA SP 3357	Low Voltage Differential Signalling
ANSI X3T11	Fibre Channel Physical Level Working draft proposed American National Standard for Information Systems, Rev. 4.3 June 1, 1994 Levels FC-0 and FC-1.

3 Explanation of Terms and Abbreviations

3.1 Terms and definitions

Headend: Equipment which is connected between receiving antennas or other signal sources and the remainder of the cable distribution system to process the signals to be distributed.

> NOTE: The headend may, for example, comprise antenna amplifiers, frequency converters, combiners, separators and generators.

SMATV: Satellite Master Antenna Television system. A system which is designed to provide sound and television signals to the households of a building or group of buildings. Two system configurations are defined in ETS 300 473 as follows:

- SMATV system A, based on transparent transmodulation of QPSK satellite signals into QAM signals to be distributed to the user
- SMATV system B, based on direct distribution of QPSK signals to the user, with two options:
  - SMATV-IF distribution on the satellite IF band (above 950 MHz)
  - SMATV-S distribution on the vhf/uhf band, for example in the extended S-band (230-470 MHz)

3.2 Abbreviations

8B/10B	eight to ten bit conversion
ASI	Asynchronous Serial Interface
BER	Bit Error Rate
LVDS	Low Voltage Differential Signalling
MSB	Most Significant Bit
PMD	Physical Medium Dependent
QAM	Quadrature Amplitude Modulation
QPSK	Quarternary Phase Shift Keying
RS	Reed Solomon
SSI	Synchronous Serial Interface
TS	Transport Stream

4 Interfaces for MPEG-2 Data Signals

4.1 Introduction

This chapter describes possible interfaces for devices transmitting or receiving MPEG-2 data as transport packets, such as QPSK demodulators, QAM modulators, multiplexers, demultiplexers, or telecom network adapters.

This specification is similar to ETS 300429 and ETS 300421.

> NOTE - Both standards describe a first functional block representing the MPEG2 source coding and multiplexing as standardised in ISO 13818-1, a second functional block representing the channel adaptation, whereas an interface in between shall be based on MPEG2 transport stream specification as per ISO 13818-1.
>
> The function of the channel modulator/demodulator is to adapt the signal to the characteristics of the transmission channel: satellite, terrestrial or cable as specified in the DVB base line documents.
>
> Also the case where data signals are transmitted to or from a headend via a telecom network or if a headend serves to insert data signals into such networks is considered to be covered by the generic channel modulator / demodulator functional block. The interface parameters valid for this network have to be met. For the latter reference is made to ITU-T G.703 for Plesiochronic Digital Hierarchy (PDH) networks.

4.1.1 Application requirements

In order to avoid any unnecessary processing at transmitting or receiving station of an interface in certain applications, it is considered an application requirement that the interface supports 204 byte packet length in such cases, in addition to or instead of the 188 packet length as specified in ISO 13818-1. These two cases are identified in the protocol diagrams of figure 1 where also the scope of this specification is delineated. The relevant associated packet structures are illustrated in figure 2.

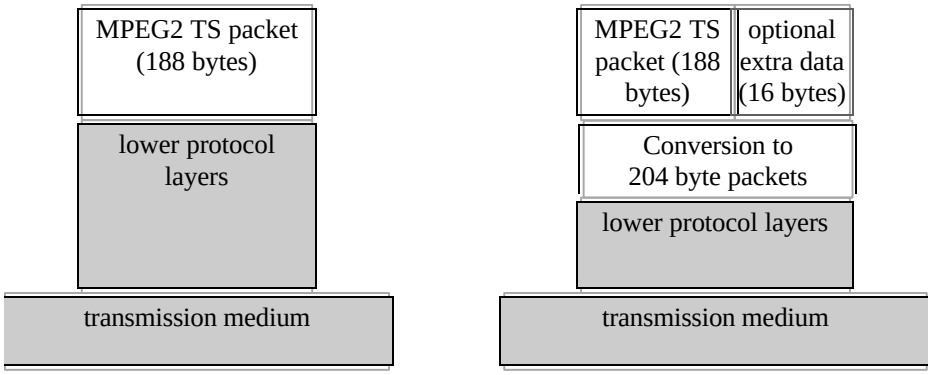


Figure 1a - protocol stack for 188 byte packets

Figure 1b - Protocol stack for 204 byte packets

(shaded areas identify the scope of this specification)

Figure 1 - Protocolstacks

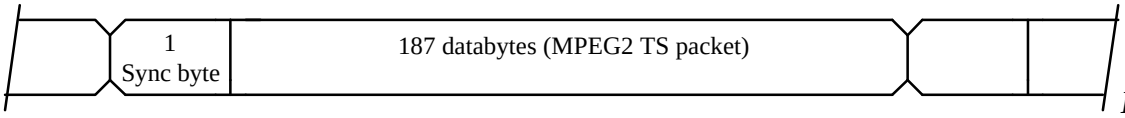


Figure 2a - packet structure of 188 byte packet

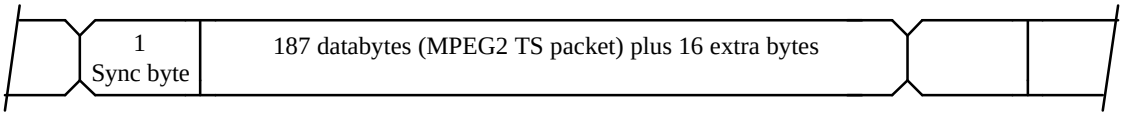


Figure 2b - Packet structure of 204 byte packet

Figure 2 - Packet structures

4.1.2 Interfaces

Three interfaces and two serial transmission media are specified as follows:
- SPI (Synchronous Parallel Interface);
- SSI-C (Synchronous Serial Interface on coaxial cable);
- SSI-O (Synchronous Serial Interface on optical fibre);
- ASI-C (Asynchronous Serial Interface on coaxial cable);
- ASI-O (Asynchronous Serial Interface on optical fibre).

Each of these interfaces feature a BER such that FEC is not required for reliable data transport.

The synchronous parallel interface is specified to cover short or medium distances, i.e. for devices arranged near to each other. Section 4.2 describes the definitions for such a parallel interface derived from CCIR Recommendation G.656. Flags are provided to distinguish 188 byte packets from 204 byte packets, and to signal the existence of valid RS bytes. Note that the interface as such is transparent to the RS bytes.

The synchronous serial interface (SSI) which can be seen as an extension of the parallel interface, is briefly introduced in section 4.3 and described in detail in annexes A and D. The packet length and the existence of valid RS bytes are conveyed through suitable coding mechanisms.

Section 4.4 introduces the Asynchronous Serial Interface (ASI). Details of the ASI are provided in annexes B and E. The ASI is configurable to either convey 188 byte packets (which is mandatory) or optionally 204 byte packets.

4.1.3 Packet length and contents

Each of the interface specifications can be used to convey either 188 byte packets or 204 byte packets in order to enable selection of the appropriate interface characteristics dependent on the kind of equipment to be interconnected. Which packet sizes are mandatory and which are optional is specified in table 1.

Table 1 - Mandatory and optional packet lengths

Interface		Data packet carrying capability		
		188 bytes	204 bytes (with 16 dummy bytes)	204 bytes (with 16 RS bytes)
SPI	transmitter	O	M	O
	receiver	M	M	M
SSI	transmitter	O	M	O
	receiver	M	M	M
ASI	transmitter	M	O	O
	receiver	M	O	O

M mandatory
O optional

In case the data stream is packetised in 188 byte packets and the interface is configured to convey 204 byte packets, the extra packet length can be used for additional data. The contents of the 16 bytes in this extra packet length are not specified in this standard. One application could be the transmission of 16 RS bytes associated with the preceding transport package.

4.1.4 Compliance

For an equipment to be compliant to this standard it is sufficient for the equipment to show at least one instance of at least one of the interface specifications as introduced in 4.1.2 and specified in detail in subsequent sections of this document, while at least the mandatory packet sizes as indicated in 4.1.3 shall be supported.

4.1.5 System integration

The interfaces specified in this document define physical connections between various pieces of equipment. It is important to notice that various parameters which are important for interoperation are not specified in this specification. This is intentional as it leaves maximum implementation flexibility for different applications. In order to facilitate system integration equipment suppliers shall provide the following information about the characteristics of the interfaces in their equipment:

- Interface type (SPI, SSI-C, SSI-O, ASI-C, ASI-O);
- Supported packet length (188 bytes, 204 bytes, both);
- Maximum input jitter (jitter measured as specified in ISO 13818 part 9);
- Output jitter (jitter measured as specified in ISO 13818 part 9);
- Minimum input data rate (rate measured as specified in ISO 13818 part 1);
- Maximum input data rate (rate measured as specified in ISO 13818 part 1).

Some of these parameters may not be applicable to certain types of equipment. If all relevant parameters are provided by equipment suppliers, the proper functioning of the complete system can be ensured.

4.2 Synchronous Parallel Interface (SPI)

This section describes an interface for a system for parallel transmission of variable data rates. The data transfer is synchronized to the byte clock of the data stream, which is the MPEG transport stream. Transmission links use LVDS technology and 25 pin connections.

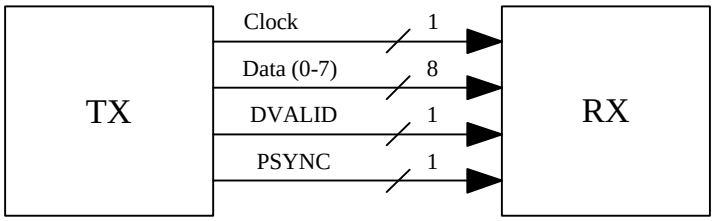


Figure 3 - System for Parallel Transmission

The data to be transmitted are MPEG-2 transport packets with 188 or 204 bytes. In the case of the 204 byte packet format packets may contain a 16 bytes "empty space", a DVALID Signal serves to identify these padding bytes. A PSYNC flag labels the beginning of a packet. The data are synchronized to the clock depending on the transmission rate.

Equipment which implements the parallel interface shall support the three transmission formats as shown in figures 4, 5 and 6.

4.2.1 Signal Format

The clock, data, and synchronization signals are transmitted in parallel: 8 data bits together with one (MPEG-2) PSYNC signal and a DVALID signal which indicates in the 204 byte mode that the empty space is filled with dummy bytes. All signals are synchronous to the clock signal. The signals are coded in NRZ form.

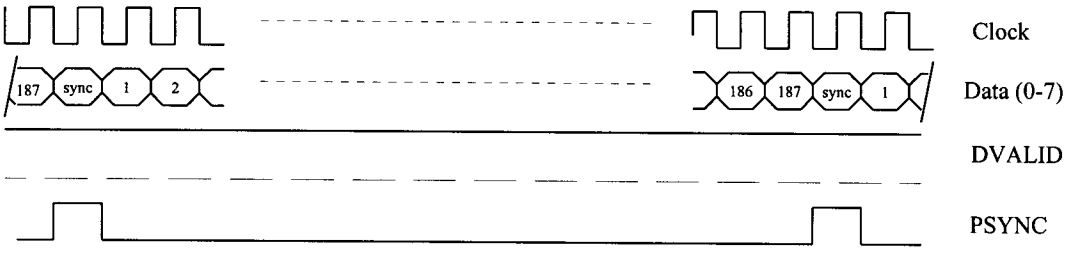


Figure 4 - Transmission Format with 188 Byte Packets

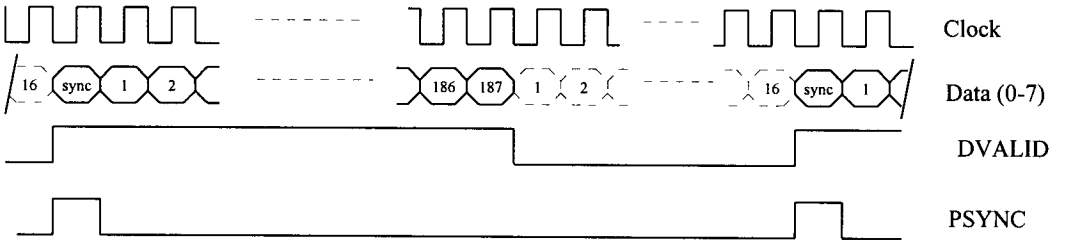


Figure 5 - Transmission Format with 204 Byte Packets (188 data bytes and 16 dummy bytes)

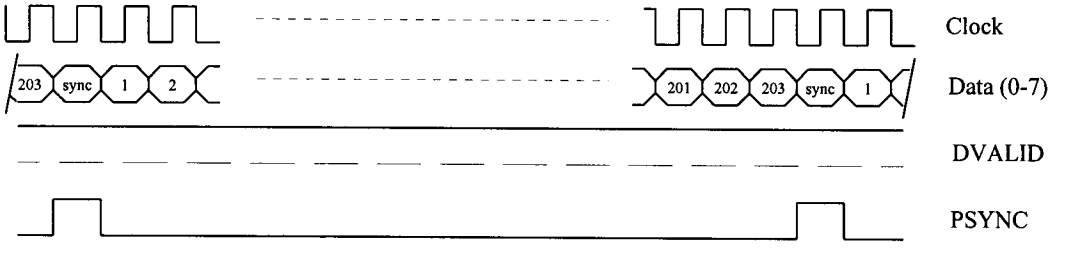


Figure 6 - Transmission Format with 204 Bytes Packets (188 data bytes and 16 valid extra bytes)

Data (0-7): Transport packet data word (8 bit: Data 0 to Data 7). Data 7 is the most significant bit.

DVALID: active logic "1". Indicates valid data at the interface. It is constantly high in the 188 byte mode. In the 204 byte mode a low logical state indicates not to check the extra (dummy) bytes.

PSYNC: active logic "1". Indicates the beginning of a transport packet by signalling the sync byte.

4.2.2 Clock Signal

The clock is a square wave signal where the 0-1 transition represents the data transfer time. The clock frequency f_p depends on the transmission rate:

- The transport packets are transmitted without insertion of additional bytes for RS coding or padding (packet length 188 bytes):

$$f_p = f_u / 8$$

- The transport packets are transmitted with insertion of additional bytes for RS coding or padding (packet length 204 bytes):

$$f_p = (204 / 188)\, f_u / 8$$

The frequency f_u corresponds to the useful bitrate R_u of the MPEG2 transport layer. The clock frequency f_p shall not exceed 13,5 MHz.

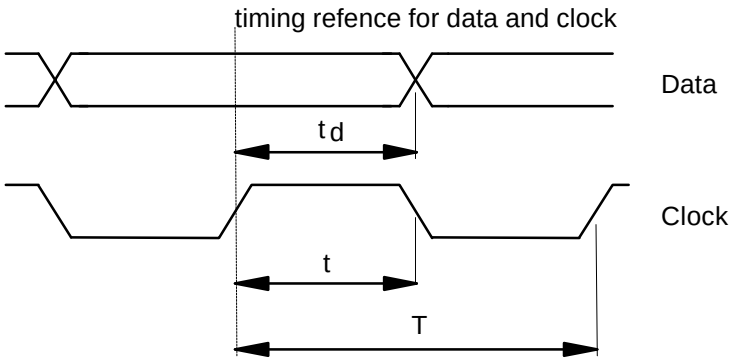


Figure 7 - Clock to Data Timing (at source)

Clock period: $T = \frac{1}{f_p}$

Clock pulse width: $t = \frac{T}{2} \pm \frac{T}{10}$

Data hold time: $t_d = \frac{T}{2} \pm \frac{T}{10}$

4.2.3 Electrical characteristics of the interface

The interface employs eleven line drivers and eleven line receivers. Each line driver (source) has a balanced output and the corresponding line receiver (destination) a balanced input (see figure 8). The line driver and receiver must be LVDS - compatible, i.e. they must permit the use of LVDS for their drivers or receivers (for details concerning LVDS, see EIA/TIA SP 3357). All digital signal time intervals are measured between the half - amplitude points.

Logic convention

The terminal A of the line driver is positive with respect to the terminal B for a binary 1 and negative for a binary 0 (see figure 8).

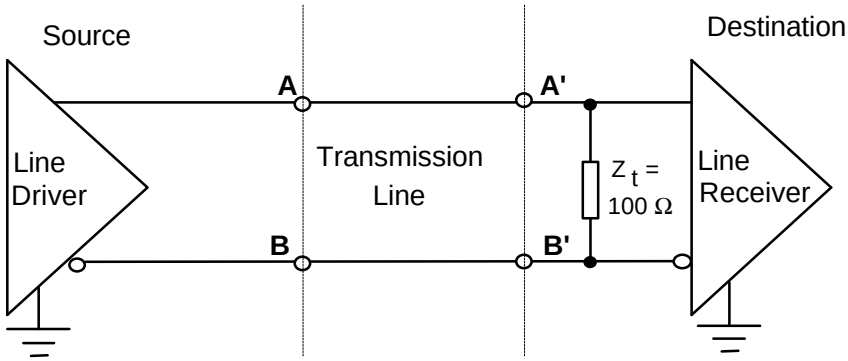


Figure 8 - Line driver and line receiver interconnection

Line Driver Characteristics (Source)

Output impedance:	100 Ω maximum
Common mode voltage:	1,125 V to 1,375 V
Signal amplitude:	247 mV to 454 mV
Rise and fall times:	less than T/7, measured between the 20% and 80% amplitude points, with a 100 Ω resistive load. The difference between rise and fall times shall not exeed T/20.

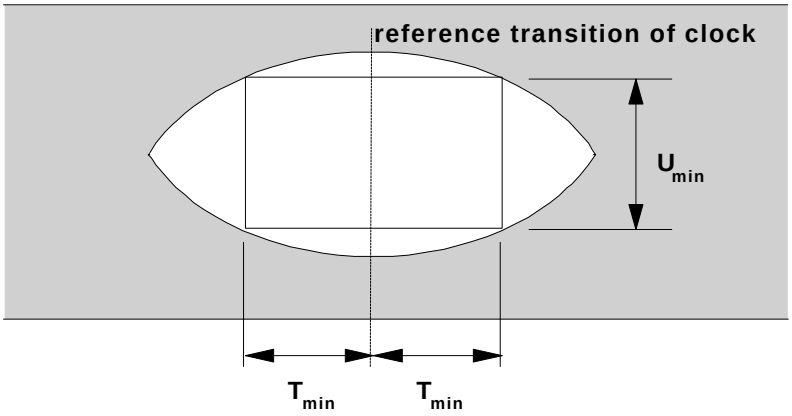
Line Receiver Characteristics (Destination)

Intput impedance:	90 Ω to 132 Ω
Maximum input signal:	2,0 V peak to peak
Minimum input signal:	100 mV peak to peak

However, the line receiver must sense correctly the binary data when a random data signal produces the conditions represented by the eye diagram in figure 9 at the data detection point.

Maximum common mode signal: ± 0,5 V, comprising interference in the range of 0 to 15 kHz (both terminals to ground).

Differential delay: Data must be correctly sensed when the clock - to - data differential delay is in the range between ± T/3 (see figure 9).



T_{min} = T/3, U_{min} = 100 mV

Figure 9 - Idealized Eye Diagram corresponding to the Minimum Input Signal Level

4.2.4 Mechanical details of the connector

The interface uses the 25 contact type D subminiature connector specified in ISO Document 2110 (1989), with the contact assignment shown in table 1.

Connectors are locked together with a screw lock, with a male screw on the cable connector and a female threaded posts on the equipment connector. The threads are of type UNC 4-40. Cable connectors employ pin contacts and equipment connectors employ socket contacts. Shielding of the interconnecting cable and its connectors must be employed.

Table 1 - Pin Assignment

Pin	Signal line	Pin	Signal line
1	Clock A	14	Clock B
2	System Gnd	15	System Gnd
3	Data 7 A(MSB)	16	Data 7 B
4	Data 6 A	17	Data 6 B
5	Data 5 A	18	Data 5 B
6	Data 4 A	19	Data 4 B
7	Data 3 A	20	Data 3 B
8	Data 2 A	21	Data 2 B
9	Data 1 A	22	Data 1 B
10	Data 0 A	23	Data 0 B
11	DVALID A	24	DVALID B
12	PSYNC A	25	PSYNC B
13	Cable Shield		

4.3 Synchronous Serial Interface (SSI)

The Synchronous Serial Interface (SSI) can be seen as the extension of the parallel interface by means of an adaptation of the parallel format. SSI is synchronous to the transport stream which is transmitted on the serial link.

A detailed specification of the SSI is provided in normative Annex A and guidelines for its implementation are provided in informative Annex D.

4.4 Asynchronous Serial Interface (ASI)

The Asynchronous Serial Interface (ASI) is a serial link operating at a fixed line clock rate.

A detailed specification of ASI is provided in normative Annex B and guidelines for its implementation are provided in informative Annex E.

Annex A (normative): Synchronous Serial Interface (SSI)

This annex describes a system for serial, encoded transmission of different data rates with a transmission rate equal to the data rate. It is based on a layered structure of MPEG-2 Transport Packets as a top layer (layer 2), and a pair of bottom layers attached to physical and coding aspects (layer 0 and layer 1).

The SSI is based on a line rate directly locked to the transport rate. The SSI is functionally equivalent to the parallel interface since the transport packets can be transmitted either contiguously or separated by 16 bytes reserved for dummy bytes or extra bytes. Because the link and the TS stream are synchronous, the bit justification operation is not needed. The system shall be designed to fulfil the high stability requirements of the modulator clocks, even when several links are cascaded.

As an example, consider a signal which passes through several re-broadcast steps, such as the one depicted in figure A1. In this chain, the last clock (that of the QAM modulator) is slaved to the encoder/mux clock via four steps of clock regeneration circuits.

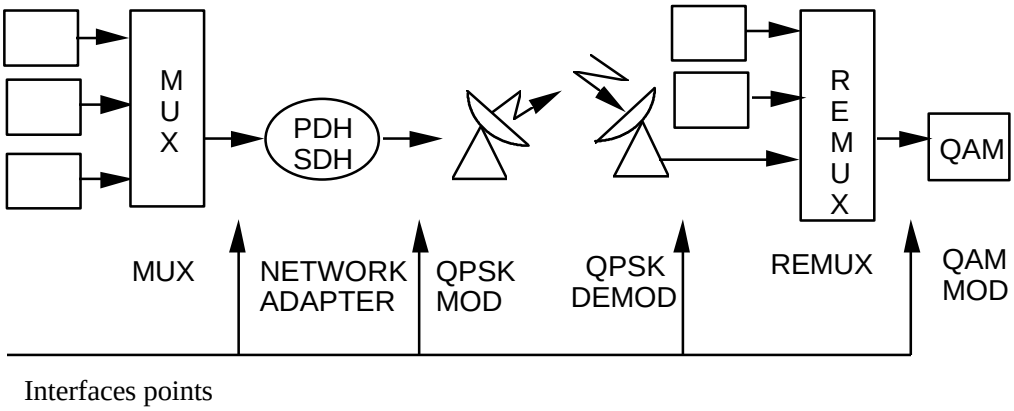


Figure A1 - An example of cascaded interfaces

A1 SSI Transmission System Overview

Figures A2 and A3 represent the primary components of this SSI method over copper coaxial cable and fibre-optic cable, respectively.

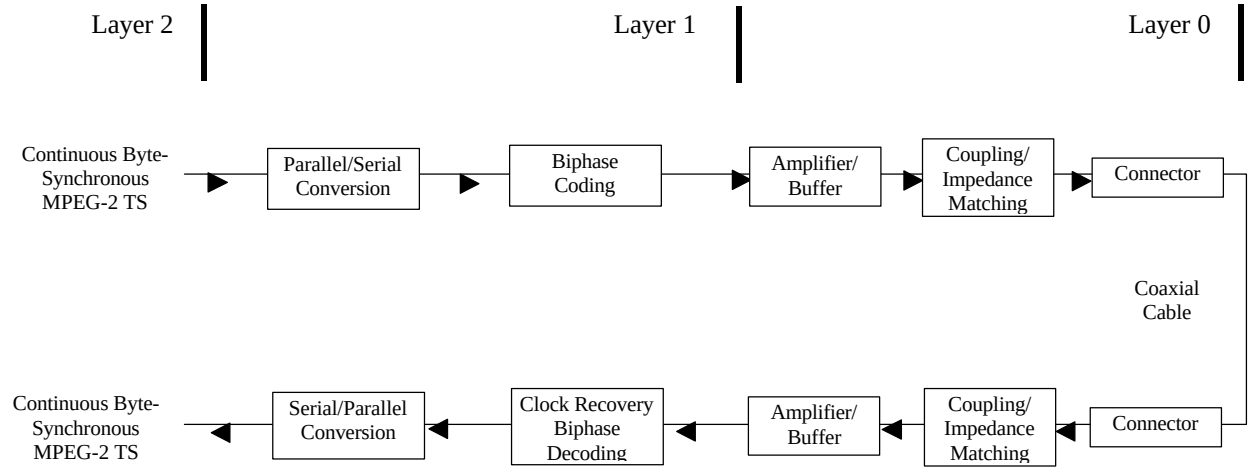


Figure A2 - Coaxial Cable-based Serial Transmission Link (SSI-C)

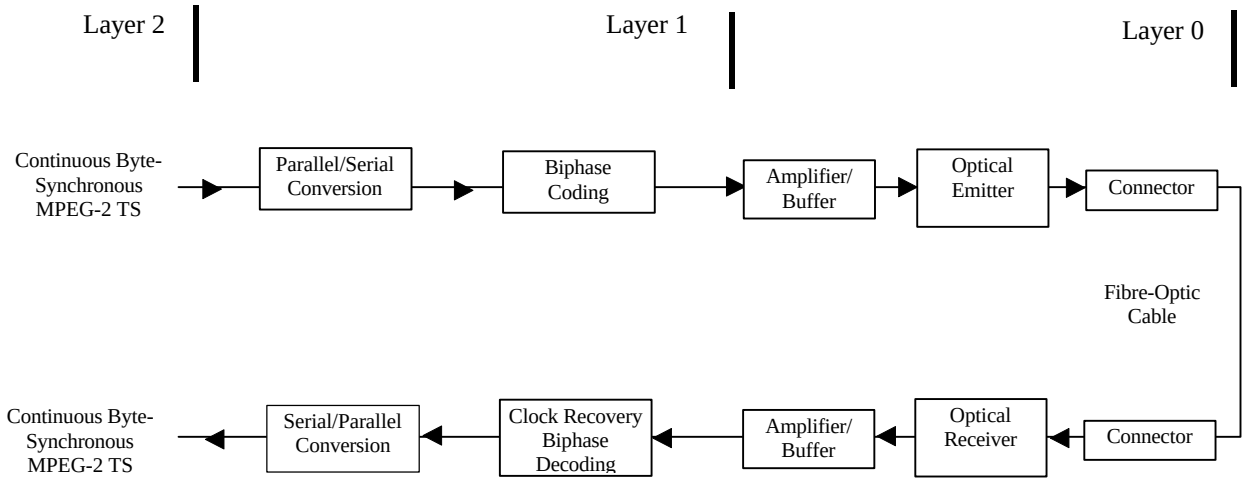


Figure A3 - Fibre-Optic-based Serial Transmission Link (SSI-O)

The main functions of the transmission system are described below.

Emission path

Data to be transmitted are presented in byte-synchronised form as MPEG-2 Transport Packets. The Transport Stream is then passed through a parallel-to-serial converter. The line data stream is locked to the TS data stream.

The serial signal is Biphase Mark encoded.

In the case of a coaxial cable application, the resulting signal is typically passed to a buffer/driver circuit and then through a coupling network, which performs impedance matching and optionally galvanic isolation, to a coaxial connector. In the case of fibre-optic application, the serial bit stream is passed through a driver circuit which drives an optical transmitter (LED or LASER) which is coupled to a fibre optic cable through a connector.

Reception path

The incoming data stream from the coaxial cable is first coupled through a connector and coupling network to a circuit which recovers clock and data. In case of fibre-optic transmission, a light sensitive detector converts light levels to electrical levels which then passed to a clock and data recovery circuit.

Once the clock and data are recovered, the bit stream is passed to a Biphase decoder. In order to recover byte alignment, a decoder searches in the serial stream for the synchronisation word which is necessary to achieve the serial to parallel conversion.

Annex D provides further clarification of the characteristics of the SSI and implementation guidelines for clock and data recovery.

A2 SSI Configuration

A SSI Interconnection physically consists of two nodes: a transmitting node and a receiving node. This unidirectional optical fibre or copper coaxial cable carrying data from the transmitting node to the receiving node is referred to as a link. The link is used by the interconnected ports to perform communication. Physical equipment such as video or audio compressors, multiplexers, modulators, etc., can be interconnected through these links. This SSI specification section applies only to the point-to-point type link.

A3 SSI Protocol Architecture Description

The SSI protocol is divided into three architectural layers for purposes of development of the standard: Layer-0, Layer-1, Layer-2.

A3.1 Layer-0: Physical Requirements

The physical layer defines the transmission media, the drivers and receiver. The transmission uses biphase mark encoding.

This section provides specifications for SSI physical layer (layer-0). Interfaces for coaxial and optical fibre applications are specified. The links are unidirectionnal point to point.

A3.1.1 Coaxial Cable Physical Medium Dependent specification

The cable impedance shall be nominally 75 ohm.

Considering that the transmission data rate is derived from the user data rate, longer links can be achieved for lower user data rates. The physical medium specified in this section has the following caracteristics:

- Provide a means of coupling the SSI Layer-1 to the coaxial cable segment
- Provide the driving of coaxial cable between a transmitter and a receiver
- Specifies the type and grade of cable and connectors to be used in a DVB Serial Interface link.

Electrical Medium Connector

The required connector shall have mechanical characteristics conforming to the BNC type. Electrical characteristics of the 75 ohm connector shall permit it to be used at frequencies up to 850 MHz.

The following table A1 and figures A4 and A5 give the requirements for the serial signal launched synchronously on the coaxial cable.

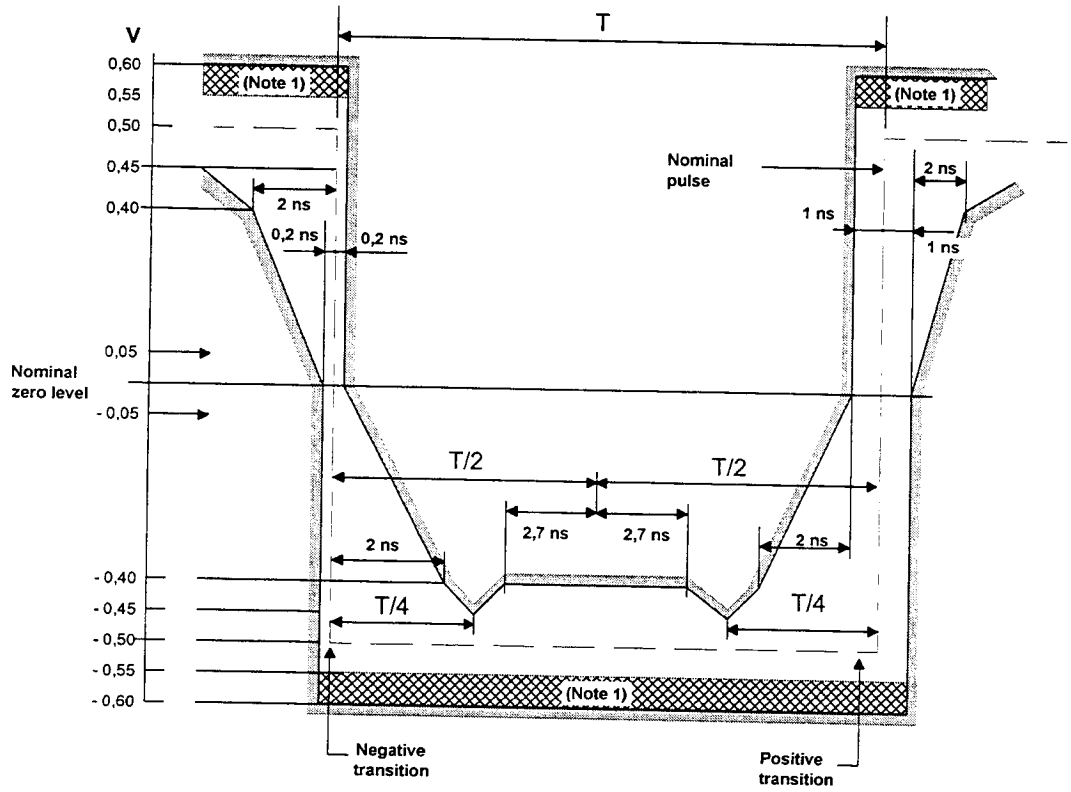
Table A1 - Transmitter output characteristics

Pulse Shape	Nominally rectangular and conforming to masks shown in figures A4 and A5.
Peak to peak voltage	1 V ± 0,1 V
Rise/Fall Time (10-90%)	£ 4 ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transition)	Negative transition: ± 0,2 ns Positive transition at unit interval boundaries: ± 1 ns Positive transition at mid interval: ± 0,7 ns
Return loss	- 15 dB over frequency range 3,5 MHz to 105 MHz
Maximum peak-to peak jitter at the output port	2 ns

The digital signal presented at the input port shall conform to table A2 and figures A4 and A5 modified by the characteristics of the interconnecting coaxial pair. The attenuation of the coaxial pair shall be assumed to follow an approximate $\sqrt{f}$ law. The cable shall have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

Table A2 - Receiver input characteristics

Input sensitivity	- 12 dB at a frequency of 70 MHz assuming a $\sqrt{f}$ law
Maximum peak to peak jitter at the input port	4 ns
Return loss	- 15 dB over frequency range 3,5 MHz to 105 MHz



Note 1 - The maximum "steady state" amplitude should not exceed the 0,55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0,55 V and 0,6 V, provided that they do not exceed the steady state level by more than 0,05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

Note 2 - For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0,02 μF (for data rate = 70 Mbit/s), to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0,05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0,05 V of the nominal zero level of the masks.

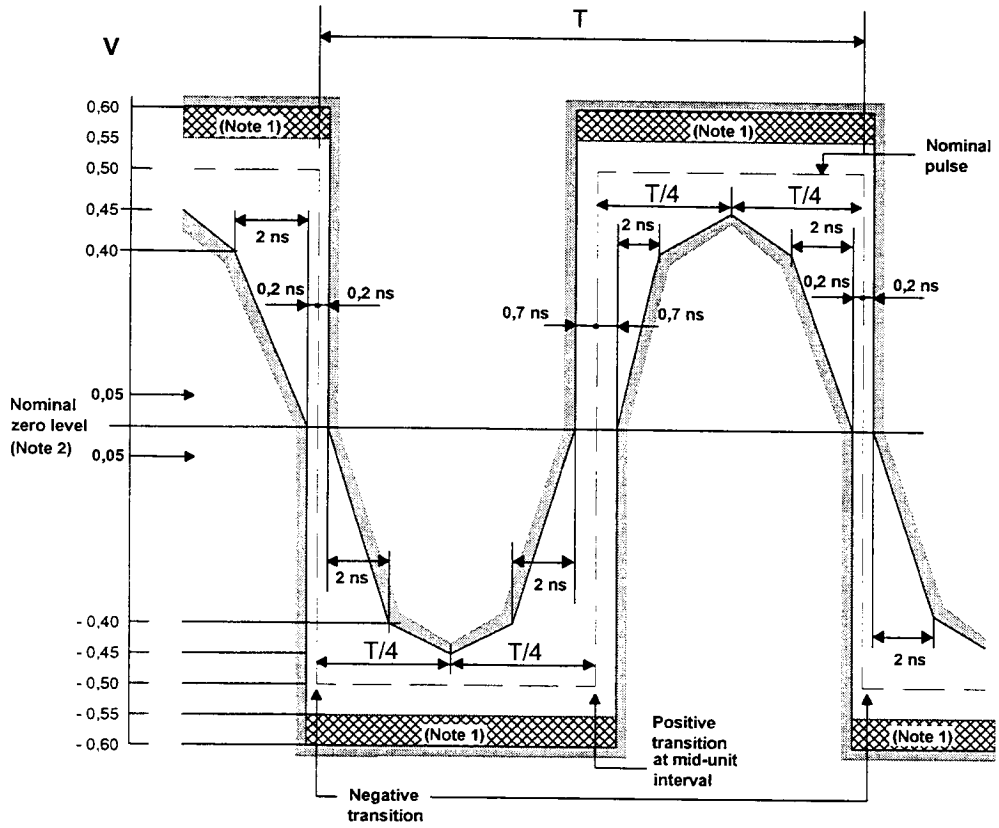
Note 3 - Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter present in the timing signal associated with the source of interface signal

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [such as a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal]. These techniques require further study.

Note 4 - For the purpose of these masks, the rise time and decay time should be measured between –0,4 V and 0,4 V, and should not exceed 4 ns.

Note 5 - The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ± 0,2 ns and ± 1 ns respectively.

Figure A4 - Pulse mask for logical 0



Note 1 - The maximum "steady state" amplitude should not exceed the 0,55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0,55 V and 0,6 V, provided that they do not exceed the steady state level by more than 0,05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

Note 2 - For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0,02 μF (for data rate = 70 Mbit/s), to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0,05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0,05 V of the nominal zero level of the masks.

Note 3 - Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by, several techniques [such as a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal]. These techniques require further study.

Note 4 - For the purpose of these masks, the rise time and decay time should be measured between -0,04 V and 0,4 V, and should not exceed 4 ns.

Figure A5 - Pulse mask for logical 1

A3.1.2 Fiber Optic Physical Medium Dependent Requirement

Transmission of the SSI data stream on fiber optic medium consists of interconnecting transmitter and receiver by a section of optical fiber which can be either multimode or singlemode type. The type of the optical fiber will be determined by the link characteristics, length and type of optical connectors.

The fibres to be used for the serial data interface are specified by CCITT Recommendations:

Multimode Fiber: CCITT Rec G.651
Singlemode Fiber: CCITT Rec G.652 or G.654

The optical connector shall be an SC type.

The optical characteristics of the links are described in the table A3. All parameters shall be met over the temperature, voltage, and lifetime range of the system.

Table A3 - Optical characteristics for SSI links

Application	intra-office	inter-office		
		Short-haul	Long-haul	
Source nominal wavelength (nm)	1310	1310	1310	1550
Type of fibre	Rec G 651	Rec G 652	Rec G 652	Rec G 652 Rec G 654
Distance (km)	< 2	< 15	< 40	< 60

Transmitter				
Source type	LED	Laser Diode	Laser Diode	DFB Laser Diode
Mean launched power (dBm)				
max	-8	-8	-8	0
min	-15	-15	-15	-5

Receiver				
minimum sensitivity (dBm)	-23	-28	-34	-34
minimum overload (dBm)	-8	-8	-10	-10
Maximum optical path penalty (dB)	1	1	1	1

A3.2 Layer 1: Data Encoding

The SSI layer 1 deals with encoding/decoding aspects which are independent of the transmission medium characteristics. Furthermore, this first layer performs the recognition of the three different transmission formats (see figures 4, 5 and 6) in order to allow a fully transparent serialisation / deserialisation.

Layer-1 operations consist of
- distinguishing the three transmission formats;
- a parallel to serial conversion of the 8-bit byte with the MSB transmitted first;
- biphase coding of the serial signal in the transmitter.

The inverse operations are performed in the receiver.

Distinction between the three transmission formats is performed as follows:
- the transmission format with 188 byte packets (figure 4) is characterized by a synchronisation byte 47H, the periodicity of which is 188 bytes;
- the transmission format with 204 byte packets with 16 dummy bytes (figure 5) is characterized by a synchronisation byte 47H, the periodicity of which is 204 bytes;
- the transmission format of packets of 204 bytes with valid extra bytes (figure 6) is characterized by an inverted synchronization byte (B8H) the periodicity of which is 204 bytes.

Line Coding

A biphase-mark code shall be used. Figure A6a describes the rules of biphase-mark coding whereas figure A6b illustrates that the required medium bandwidth is twice the bandwidth required by NRZ coding.

The encoding rules are as follows:
- a transition always occurs at the beginning of the bit whatever its value is (0 or 1).
- for logical 1, a transition occurs in the middle of the bit
- for logical 0, there is no transition on the middle of the bit.

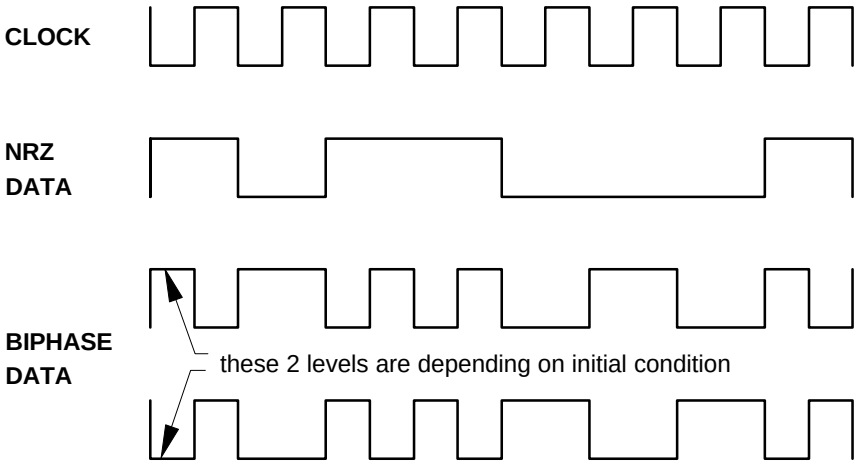


Figure A6a - Biphase mark coding scheme

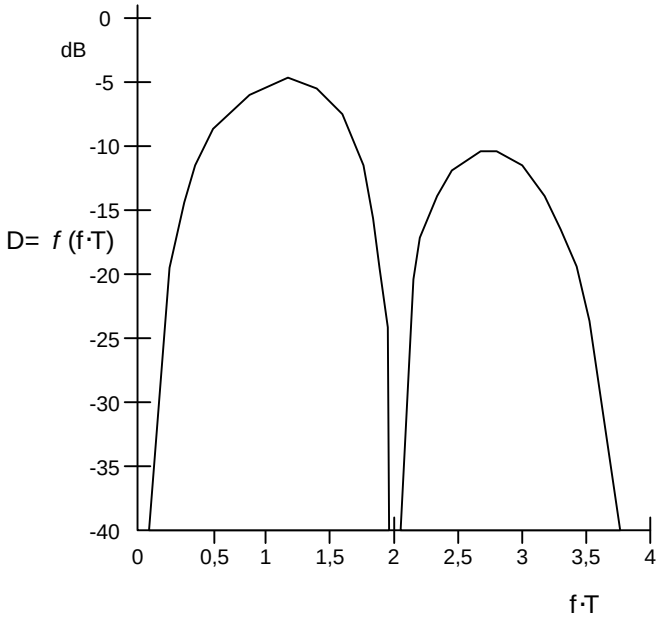


Figure A6b - Spectral density of biphase code (T is the bit duration of NRZ data)

Figure A6 - Biphase Mark encoding

Byte synchronisation

The byte synchronisation process in the receiving equipment has to take into account the two possible packet formats, i.e. the 188 byte-packet format and the 204 byte-packet format. The packet synchronisation word (47H or B8H) is used as a byte alignment pattern which serves for initializing the serial to parallel conversion. The occurrence of the synchronisation byte (188 bytes or 204 bytes) and the value of the synchronisation byte (47H or B8H) are used to restore the DVALID signal and the PSYNC signal.

If the received transmission format is the 204 byte packet with valid extra bytes as indicated in figure 6, the synchronisation byte (B8H) must be inverted in order to recover the original synchronisation byte (47H) of the TS packet format to be delivered to layer 2.

> NOTE - In order to prevent possible synchronisation errors, it is recommended that consecutive bytes 47H do not occur within the 188 byte or 204 byte data packet.

Clock recovery

In the receiver the clock recovery circuit extracts the transport clock directly from the encoded data stream. The clock corresponds directly to the user data rate.

Bit-Error-Rate (BER) Requirement

The BER shall be less then one part in 10^{13}, as measured where data pass from layer-1 to layer-2. That is, BER shall be measured where data emerge from the Biphase-Mark decoder.

A3.3 Layer 2: Transport protocol

The SSI layer-2 uses the MPEG-2 Transport Stream Packet as defined in ISO/IEC 13818-1 (Systems) as its basic message unit. The MPEG-2 Transport Packet synchronization word (47H) is included in this Layer-2 packet definition to allow receive equipment to achieve synchronization.

The transport packets shall be presented to layer-2 either as contiguous 188 byte packets, or separated by 16 padding bytes, or contiguous 204 Reed Solomon encoded packets.

Annex B (normative): Asynchronous Serial Interface (ASI)

This annex describes a system for a serial, encoded transmission of different data rates with a constant transmission rate, based on a layered structure of MPEG Transport Packets as a top layer (Layer 2), and a pair of bottom layers based upon the Fibre Channel Standard (Layers 1 and 0).

Transport streams from different sources may have different data rates. The use of a constant transmission rate permits a constant receiver clock. To restore the original clock rate, a PLL circuit can be used. Annex E gives some proposals for how such a circuit can be designed. The input of the required transmission facility accepts MPEG-2-Bytes and the output delivers MPEG-2 Bytes.

Layer 2 is defined using the MPEG-2 Standard ISO/IEC 13818-1 (Systems). Layers 1 and 0 are based upon a subset of ANSI Standard X3T11 / Levels FC-1 and FC-0.

While the Fibre-Channel (FC) standard supports single mode fibre, multi-mode fibre, coaxial cable and twisted pair media interfaces, this document defines only two distinct forms of interfaces: coaxial cable and multi-mode fibre-optical cable using LED emitters.

Instead of a transmission rate of 265,625 Mbit/s, as required in the ANSI Standard, in this document the transmission rate is 270,000 Mbit/s.

B1 ASI Transmission System Overview

Figures B1 and B2 represent the primary components of the ASI transmission method over copper coaxial cable and fibre-optic cable, respectively.

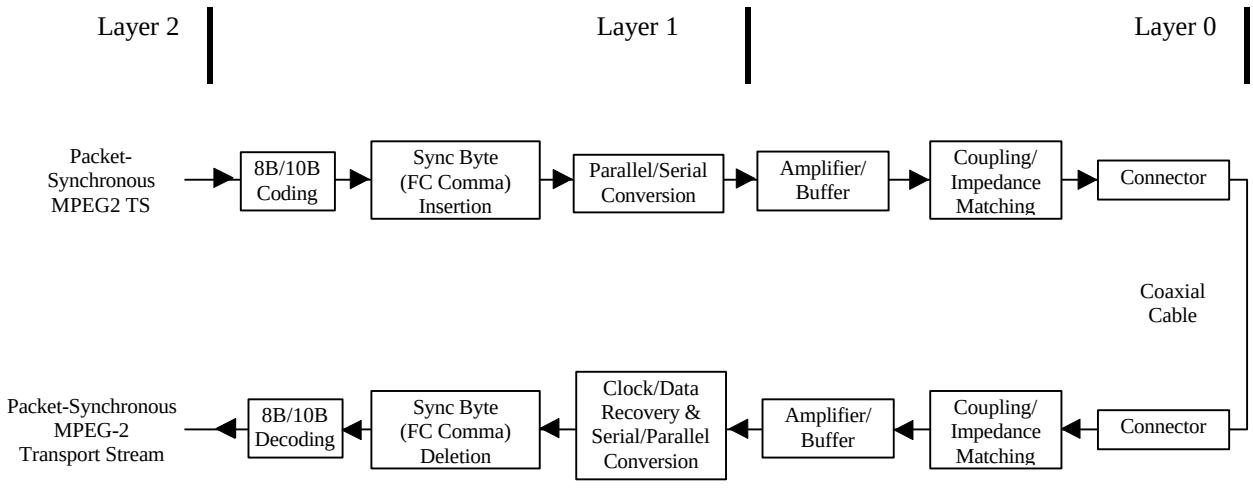


Figure B1 - Coaxial Cable-based Asynchronous Serial Transmission Link

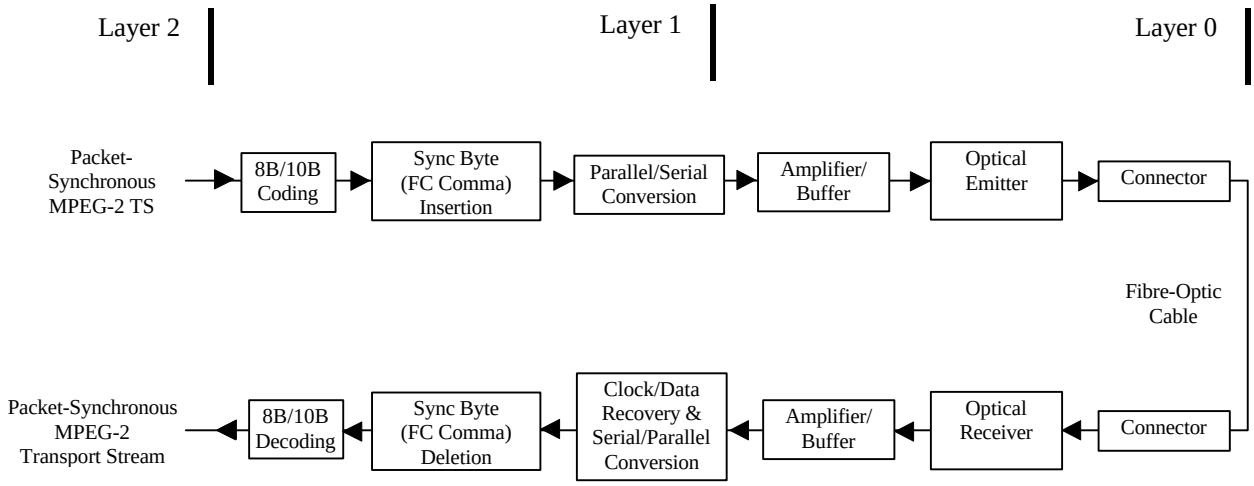


Figure B2 - Fibre-optic-based Asynchronous Serial Transmission Link

Data to be transmitted are presented in byte-synchronized form as MPEG-2 Transport packets. Bytes are then 8B/10B coded which produces one 10-bit word for each 8-bit byte presented. These 10-bit words are then passed through a parallel-to-serial converter which operates at a fixed output bit-rate of 270 Mbit/s. If the parallel-to-serial converter requests a new input word and the data source does not have one ready, a synchronization word shall inserted. These sync words are to be ignored by receive equipment. In the case of coaxial cable application, the resulting serial bit stream is typically passed to a buffer/driver circuit and then through a coupling network to a coaxial connector. In the case of fibre-optic application, the serial bit-stream is passed to a driver circuit which drives an LED emitter which is coupled to a fibre optic cable through a mechanical connector.

Receive data arriving on a coaxial cable are first coupled through a connector and coupling network to a circuit which recovers clock and data. In the case of fibre-optic transmission, a light-sensitive detector converts light levels to electrical levels which are then passed to a clock and data recovery circuit.

Recovered serial data bits are passed to an 8B/10B decoder which converts the 10-bit transmission words back into the 8-bit bytes originally transmitted. In order to recover byte alignment, the 8B/10B decoder initially searches for synchronization words; the synchronization word is a unique 10-bit pattern which is prevented from occurring (by the 8B/10B encoder) with all possible input data bytes. Once found, the start of the synchronization word marks the boundary of subsequent received data words and establishes proper byte-alignment of decoder output bytes.

B2 ASI Configuration

An ASI interconnect physically consists of two nodes: a transmitting node and a receiving node. This unidirectional optical fibre or copper coaxial cable carrying data from the transmitting node to the receiving node is referred to as a link. The link is used by the interconnected ports to perform communication. Physical equipment such as video or audio

compressors, multiplexers, modulators, etc., can be interconnected through these links. This ASI specification section applies only to the point-to-point type link.

B3 ASI Protocol Architecture Description

The ASI protocol is divided into three architectural Layers for purposes of development of the standard: Layer-0, Layer-1, and Layer-2.

B3.1 Layer-0: Physical Requirements

The physical Layer defines the transmission media, the drivers and receivers, and the transmission speeds. The physical interface provides for both LED-driven multimode fibre and copper coaxial cable. The base speed of the standard is defined at 270 Mbit/s (transmission channel speed). The basic unit of Layer-0 is the link. The points where conformance is required are shown as point S and R in the figure B3.

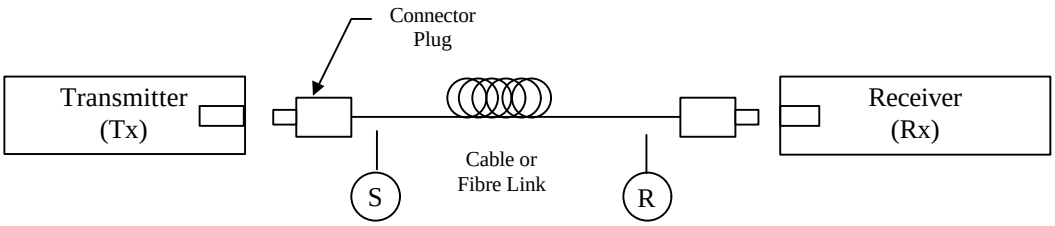


Figure B3 - Serial Link Layer-0 Reference Points

In coaxial applications, jitter is specified in the traditional manner of random and data dependent jitter and duty cycle distortion. In LED-driven fibre based applications, jitter is specified in terms of Random Jitter (RJ) and Deterministic Jitter (DJ). Deterministic jitter is the sum of data dependent jitter and duty cycle distortion. The DJ is due to the timing distortions caused by normal circuit effects in the transmission system. It comprises of propagation delay difference between the rising and falling edge of a signal and interaction of limited bandwidth of the transmission components and the symbol sequence. The RJ is due to the thermal noise in the system and usually modeled as a Gaussian process.

Line Rates and Bit Timing

The encoded line rate with the 8B/10B block code is 270 Mbit/s which results in a media transmission rate of 270 Mbaud. At the transmitter the serialization is done using a fixed oscillator to establish this 270 Mbaud rate from which a phase-locked byte clock is derived and used to shift in parallel bytes.

Receivers recover the serial transmission clock generally by the use of a phase-locked-loop (PLL) oscillator locked to bit transitions of the incoming data stream. A phase-locked byte clock is derived from this recovered serial bit clock and is used to shift parallel bytes out to Layer-1 processing elements.

It is required that the encoded line rate shall be 270 Mbaud ± 100 ppm.

Receiver Timing Acquisition

A receiver must first acquire bit synchronization, before attempting to align received bytes. This time is measured from receipt of a valid input to the time the receiver is synchronized to the bit stream and delivering valid re-timed data within the BER objective of the system.

It is required that bit synchronization shall occur in not more than 1 ms.

B3.1.1 Electrical Medium Characteristics

The cable impedance shall be nominally 75 ohm.

Electrical Medium Connector

The required connector shall have mechanical characteristics of the BNC type. Electrical characteristics of the 75 ohm connector shall permit it to be used at frequencies up to 850 MHz.

Electrical Characteristics

The parameters shall be met over the temperature, voltage and lifetime range of the system. Electrical measurements shall be made with the interface terminated with the connector specified above into 75 ohm resistive termination. Full electrical details are provided in table B1.

Table B1 - Electrical characteristic specifications for ASI link

Transmitter Output Characteristics	Units	
Output voltage	mV (p-p)	800 ± 10%
Deterministic Jitter	% (p-p)	10
Random Jitter	% (p-p)	8
Rise/Fall Time (20-80%)	ns (max)	1,2

Receiver Input Characteristics	Units	
Min Sensitivity (D21.5 idle pattern)	mV	200
Max Input Voltage	mV(p-p)	880
s_{11} (range: 0,1 to 1,0 x bit rate)	dB	-17
Min Discrete Connector Return Loss (5 MHz - 270 MHz)	dB	- 15

The interface shall be coupled to the coax via a transformer.

As measured according to the diagram in Figure B4, the eye opening provided by the transmitter shall be within the mask depicted in Figure B5.

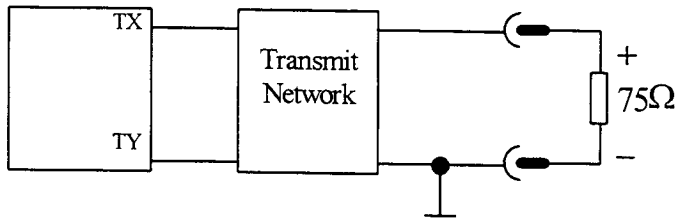


Figure B4 - Coaxial transmitter test circuit

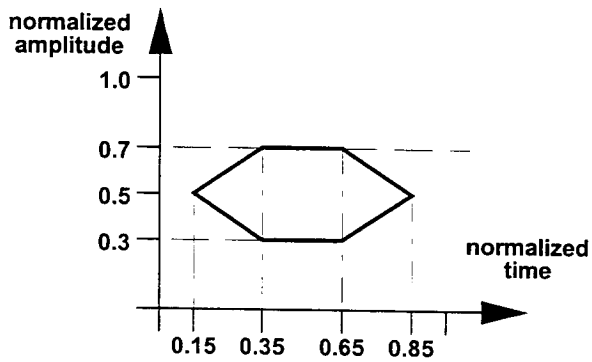


Figure B5 - Transmitter Eye Diagram for jitter

B3.1.2 Fibre Optic Medium Characteristics

The fibre optic medium consists of a single section of fibre-optic cable connecting a transmitter and receiver. The optical medium requirements are satisfied by the 62,5/125 micron nominal diameter fibre specified by IEC 793-2, type A1b, with the exceptions noted below. The system can operate, subject to certain restrictions, with a variety of optical fibres; however, performance to this specification and interoperability between vendors equipment is assured only through the use of the optical fibre specified in this section. This specification was developed on the basis of an attenuation value of less than or equal to 1,5 dB/km, when measured at a wavelength of 1300 nm. Higher loss fibre may be used for shorter fibre cable lengths.

Each optical fibre shall have a zero dispersion wavelength in the range of 1295 nm to 1365 nm and a dispersion slope not exceeding 0,110 ps/nm^2-km. Each optical fibre shall have a dispersion characteristic in the range shown in table B2 below:

Table B2 - Chromatic Dispersion Requirements:

Zero Dispersion Wavelength Lambda(0) (nm)	Maximum Dispersion slope S(0) (ps/nm^2-km)
1295-1300	[Lambda(0)-1190]/1000
1300-1348	0,110
1348-1365	[1458-Lambda(0)]/1000

Optical Medium Connector

Fibre-optic cable connectors shall be of SC type.

The optical connector shall have a maximum insertion loss of 1 dB. Connectors with different loss characteristic may be used as long as any additional loss is compensated for elsewhere in the fibre loss budget.

Optical Characteristics

The transmit interface and receive interface parameters for 270 Mbit/s multimode fibre interface shall be as summarized below. The parameters shall be met over the temperature, voltage, and lifetime range of the system. Optical measurements shall be made with the cable terminated with the optical connector and the optical fibre specified above. Fibre length shall be sufficient to ensure equilibrium mode distribution. Typically fibres require 1 to 5 meters of length to establish equilibrium mode distribution.

The complete specification is given in the following table B3 and associated figure B6.

Table B3 - Optical characteristic specifications for ASI link

Fibre Link Parameters	**Units**	
Fibre Core Diameter	µm	62,5

Transmitter Parameters	**Units**	
Type		LED
Spectral Center Wavelength	nm (min)	1280
	nm (max)	1380
Spectral Width	nm RMS (max)	NA
	nm FWHM (max)	See figure B6
Launched Power, max	dBm (ave)	-14
Launched Power, min	dBm (ave)	-20
Extinction Ratio	dB (min)	9
RIN_{12} (max)	dB/Hz	NA
Eye Opening @ BER=10^{-12}	% (min)	NA
Deterministic Jitter	% (p-p)	16
Random Jitter	% (p-p)	9
Optical Rise/Fall Time	ns (max)	2,0/2,2

Receiver Parameters	**Units**	
Received Power, min	dBm (ave)	-26
Received Power, max	dBm (ave)	-14
Return Loss of Receiver	dB (min)	NA
Deterministic Jitter	% (p-p)	19
Random Jitter	% (p-p)	9
Optical Rise/Fall Time	ns (max)	3,0

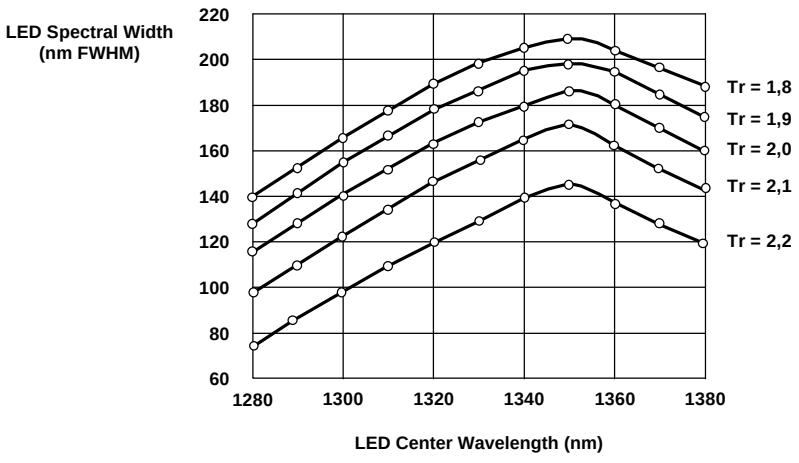


Figure B6 - Spectral Transmitter Width

B3.2 Layer-1 Data Encoding

The ASI transmission protocol includes serial encoding rules, special characters, and error control. It uses a DC balanced 8B/10B transmission code. The code maps each 8-bit data byte into a 10-bit code with the following properties: a run length of 4 bits or less and minimal DC offset. This code provides error checking through both invalid transmission code points and the notion of 'running' disparity.

Special characters are defined as extra code points beyond the need to encode a byte of data. One in particular, the comma character (K28.5 in the tables of Annex C) is used to establish byte synchronization in the ASI transmission link.

Coding Requirements

The ASI Transmission Layer 1 deals with encoding/decoding aspects which are independent of the transmission medium characteristics. At Layer-1, 8B/10B transmission coding is employed which provides for both a self checking capability and byte synchronization of the link. The 10B transmission code is defined in terms of "disparity": the difference in the number of "1" bits and "0" bits in the transmitted serial data stream. It is through the disparity characteristics of the code that DC balance is maintained. Each 8B code point has two entries in the 10B code point map corresponding to the positive and negative disparity representation for that 8B code point. The transmitter is required to maintain the running disparity of the transmitted serial bit stream within +/-1 of a neutral point by selection of the appropriate positive or negative disparity representation of the 10B code to be transmitted. The receiver will check the incoming bit stream for proper running disparity and invalid 10B code points to ensure byte level data integrity.

Line coding

The 8B/10B transmission code specified in the fiber channel document X3T11 shall be the encoding method utilized in ASI Interface Layer-1. Annex C is a reproduction of the 8B/10B coding table from that standard and a brief description of the coding process. X3T11 shall be the required standard, Annex C is for convenient reference only.

> NOTE - The ASI coding is not invariant to logical inversion of the transmitted bits. Therefore, to ensure correct operation, care must be taken that equipment interface circuitry of the non-inverting type is used.

Byte Synchronization

The byte alignment synchronization pattern shall be the K28.5 code of the 8B/10B code. The receiver shall present a properly aligned byte stream after the receipt of two K28.5 special characters aligned on the same byte boundary within a 5 byte window. The first byte received after the second K28.5 shall have valid byte alignment.

Bit-Error-Rate (BER) Performance

The BER shall be less than one part in 10^{13}, as measured where data pass from Layer-1 to Layer-2. That is, BER shall be measured where bytes emerge from the 8B/10B decoder.

Packet Synchronization

At least two synchronization code words (K28.5) shall immediately precede every Layer-2 Transport Packet.

B3.3 Layer-2 Transport Protocol

The ASI Transmission Layer-2 standard uses the MPEG-2 Transport Stream Packet as defined in ISO/IEC 13818-1 (Systems) as its basic message unit. Optionally the RS coded bytestructure as specified in ETS 300 429 is also supported. Transport packets can be transmitted as a block of contiguous bytes (that is, with no intervening sync bytes in the transmitted stream for a single packet) or as individual bytes with intervening sync bytes, or any combination of contiguous bytes and sync bytes. Additionally, the ASI Layer-2 protocol specifies that at least two synchronization words (K28.5) precede each transport packet.

> NOTE - The MPEG-2 Transport Packet Synchronization word (47H) is included in this Layer-2 packet definition to allow receiving equipment to achieve packet synchronization.The packet synchronization process is not a part of this ASI Transmission protocol definition.

Transport Requirements

The ASI Interface Layer-2 definition employs the MPEG-2 Transport Stream packet syntax with the additional requirement that every Transport Packet shall be preceded with at least two K28.5 synchronization characters. Although 8B/10B receivers can generally maintain synchronization (once initially synchronized) without interspersed synchronization codes, this leading sync byte requirement will allow re-sync within one transport packet in the event that a line disturbance causes loss of sync.

Transport Packet Format

Transport Packet structure shall conform to the specifications of ISO/IEC 13818-1. The optional support of 204 byte packets conforms to ETS 300 429 for Transport Stream Packets.

Transport Packet Timing

Transport Packets may be presented to Layer-2 either as a burst of contiguous bytes as shown in figure B7, or as individual bytes spread out in time as shown in figure B8. (These figures reflect the result of these types of packet delivery as seen at layer-1).

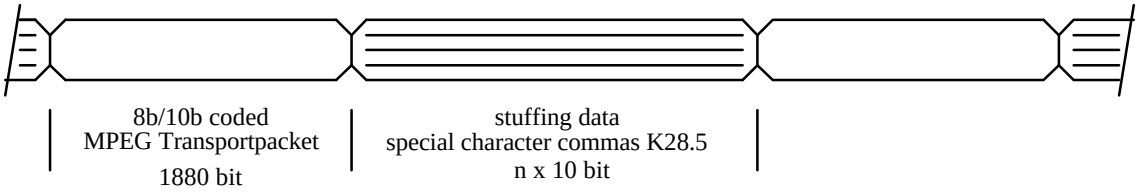


Figure B7 - Transmission Format with Data Packets (example for 188 Bytes)

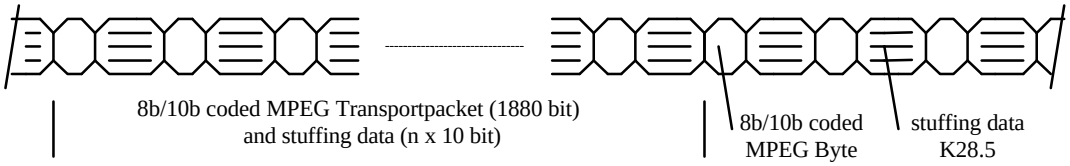


Figure B8 - Transmission Format with Data Bursts (example for 188 Bytes)

Annex C (informative): 8B/10B Tables

Data Byte Name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D0.0	000 00000	00111 0100	011000 1011	D16.1	001 10000	011011 1001	100100 1001
D1.0	000 00001	011101 0100	100010 1011	D17.1	001 10001	100011 1001	100011 1001
D2.0	000 00010	101101 0100	010010 1011	D18.1	001 10010	010011 1001	010011 1001
D3.0	000 00011	110001 1011	110001 0100	D19.1	001 10011	110010 1001	110010 1001
D4.0	000 00100	110101 0100	001010 1011	D20.1	001 10100	001011 1001	001011 1001
D5.0	000 00101	101001 1011	101001 0100	D21.1	001 10101	101010 1001	101010 1001
D6.0	000 00110	011001 1011	011001 0100	D22.1	001 10110	011010 1001	011010 1001
D7.0	000 00111	111000 1011	000111 0100	D23.1	001 10111	111010 1001	000101 1001
D8.0	000 01000	111001 0100	000110 1011	D24.1	001 11000	110011 1001	001100 1001
D9.0	000 01001	100101 1011	100101 0100	D25.1	001 11001	100110 1001	100110 1001
D10.0	000 01010	010101 1011	010101 0100	D26.1	001 11010	010110 1001	010110 1001
D11.0	000 01011	110100 1011	110100 0100	D27.1	001 11011	110110 1001	001001 1001
D12.0	000 01100	001101 1011	001101 0100	D28.1	001 11100	001110 1001	001110 1001
D13.0	000 01101	101100 1011	101100 0100	D29.1	001 11101	101110 1001	010001 1001
D14.0	000 01110	011100 1011	011100 0100	D30.1	001 11110	011110 1001	100001 1001
D15.0	000 01111	010111 0100	101000 1011	D31.1	001 11111	101011 1001	010100 1001
D16.0	000 10000	011011 0100	100100 1011	D0.2	010 00000	100111 0101	011000 0101
D17.0	000 10001	100011 1011	100011 0100	D1.2	010 00001	011101 0101	100010 0101
D18.0	000 10010	010011 1011	010011 0100	D2.2	010 00010	101101 0101	010010 0101
D19.0	000 10011	110010 1011	110010 0100	D3.2	010 00011	110001 0101	110001 0101
D20.0	000 10100	001011 1011	001011 0100	D4.2	010 00100	110101 0101	001010 0101
D21.0	000 10101	101010 1011	101010 0100	D5.2	010 00101	101001 0101	101001 0101
D22.0	000 10110	011010 1011	011010 0100	D6.2	010 00110	011001 0101	011001 0101
D23.0	000 10111	111010 0100	000101 1011	D7.2	010 00111	111000 0101	000111 0101
D24.0	000 11000	110011 0100	001100 1011	D8.2	010 01000	111001 0101	000110 0101
D25.0	000 11001	100110 1011	100110 0100	D9.2	010 01001	100101 0101	100101 0101
D26.0	000 11010	010110 1011	010110 0100	D10.2	010 01010	010101 0101	010101 0101
D27.0	000 11011	110110 0100	001001 1011	D11.2	010 01011	110100 0101	110100 0101
D28.0	000 11100	001110 1011	001110 0100	D12.2	010 01100	001101 0101	001101 0101
D29.0	000 11101	101110 0100	010001 1011	D13.2	010 01101	101100 0101	101100 0101
D30.0	000 11110	011110 0100	100001 1011	D14.2	010 01110	011100 0101	011100 0101
D31.0	000 11111	101011 0100	010100 1011	D15.2	010 01111	010111 0101	101000 0101
D0.1	001 00000	100111 1001	011000 1001	D16.2	010 10000	011011 0101	100100 0101
D1.1	001 00001	011101 1001	100010 1001	D17.2	010 10001	100011 0101	100011 0101
D2.1	001 00010	101101 1001	010010 1001	D18.2	010 10010	010011 0101	010011 0101
D3.1	001 00011	110001 1001	110001 1001	D19.2	010 10011	110010 0101	110010 0101
D4.1	001 00100	110101 1001	001010 1001	D20.2	010 10100	001011 0101	001011 0101
D5.1	001 00101	101001 1001	101001 1001	D21.2	010 10101	101010 0101	101010 0101
D6.1	001 00110	011001 1001	011001 1001	D22.2	010 10110	011010 0101	011010 0101
D7.1	001 00111	111000 1001	000111 1001	D23.2	010 10111	111010 0101	000101 0101
D8.1	001 01000	111001 1001	000110 1001	D24.2	010 11000	110011 0101	001100 0101
D9.1	001 01001	100101 1001	100101 1001	D25.2	010 11001	100110 0101	100110 0101
D10.1	001 01010	010101 1001	010101 1001	D26.2	010 11010	010110 0101	010110 0101
D11.1	001 01011	110100 1001	110100 1001	D27.2	010 11011	110110 0101	001001 0101
D12.1	001 01100	001101 1001	001101 1001	D28.2	010 11100	001110 0101	001110 0101
D13.1	001 01101	101100 1001	101100 1001	D29.2	010 11101	101110 0101	010001 0101
D14.1	001 01110	011100 1001	011100 1001	D30.2	010 11110	011110 0101	100001 0101
D15.1	001 01111	010111 1001	101000 1001	D31.2	010 11111	101011 0101	010100 0101

Table C1 - Valid Data Characters

Data Byte Name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D0.3	011 00000	100111 0011	011000 1100	D16.4	100 10000	011011 0010	100100 1101
D1.3	011 00001	011101 0011	100010 1100	D17.4	100 10001	100011 1101	100011 0010
D2.3	011 00010	101101 0011	010010 1100	D18.4	100 10010	010011 1101	010011 0010
D3.3	011 00011	110001 1100	110001 0011	D19.4	100 10011	110010 1101	110010 0010
D4.3	011 00100	110101 0011	001010 1100	D20.4	100 10100	001011 1101	001011 0010
D5.3	011 00101	101001 1100	101001 0011	D21.4	100 10101	101010 1101	101010 0010
D6.3	011 00110	011001 1100	011001 0011	D22.4	100 10110	011010 1101	011010 0010
D7.3	011 00111	111000 1100	000111 0011	D23.4	100 10111	111010 0010	000101 1101
D8.3	011 01000	111001 0011	000110 1100	D24.4	100 11000	110011 0010	001100 1101
D9.3	011 01001	100101 1100	100101 0011	D25.4	100 11001	100110 1101	100110 0010
D10.3	011 01010	010101 1100	010101 0011	D26.4	100 11010	010110 1101	010110 0010
D11.3	011 01011	110100 1100	110100 0011	D27.4	100 11011	110110 0010	001001 1101
D12.3	011 01100	001101 1100	001101 0011	D28.4	100 11100	001110 1101	001110 0010
D13.3	011 01101	101100 1100	101100 0011	D29.4	100 11101	101110 0010	010001 1101
D14.3	011 01110	011100 1100	011100 0011	D30.4	100 11110	011110 0010	100001 1101
D15.3	011 01111	010111 0011	101000 1100	D31.4	100 11111	101011 0010	010100 1101
D16.3	011 10000	011011 0011	100100 1100	D0.5	101 00000	100111 1010	011000 1010
D17.3	011 10001	100011 1100	100011 0011	D1.5	101 00001	011101 1010	100010 1010
D18.3	011 10010	010011 1100	010011 0011	D2.5	101 00010	101101 1010	010010 1010
D19.3	011 10011	110010 1100	110010 0011	D3.5	101 00011	110001 1010	110001 1010
D20.3	011 10100	001011 1100	001011 0011	D4.5	101 00100	110101 1010	001010 1010
D21.3	011 10101	101010 1100	101010 0011	D5.5	101 00101	101001 1010	101001 1010
D22.3	011 10110	011010 1100	011010 0011	D6.5	101 00110	011001 1010	011001 1010
D23.3	011 10111	111010 0011	000101 1100	D7.5	101 00111	111000 1010	000111 1010
D24.3	011 11000	110011 0011	001100 1100	D8.5	101 01000	111001 1010	000110 1010
D25.3	011 11001	100110 1100	100110 0011	D9.5	101 01001	100101 1010	100101 1010
D26.3	011 11010	010110 1100	010110 0011	D10.5	101 01010	010101 1010	010101 1010
D27.3	011 11011	110110 0011	001001 1100	D11.5	101 01011	110100 1010	110100 1010
D28.3	011 11100	001110 1100	001110 0011	D12.5	101 01100	001101 1010	001101 1010
D29.3	011 11101	101110 0011	010001 1100	D13.5	101 01101	101100 1010	101100 1010
D30.3	011 11110	011110 0011	100001 1100	D14.5	101 01110	011100 1010	011100 1010
D31.3	011 11111	101011 0011	010100 1100	D15.5	101 01111	010111 1010	101000 1010
D0.4	100 00000	100111 0010	011000 1101	D16.5	101 10000	011011 1010	100100 1010
D1.4	100 00001	011101 0010	100010 1101	D17.5	101 10001	100011 1010	100011 1010
D2.4	100 00010	101101 0010	010010 1101	D18.5	101 10010	010011 1010	010011 1010
D3.4	100 00011	110001 1101	110001 0010	D19.5	101 10011	110010 1010	110010 1010
D4.4	100 00100	110101 0010	001010 1101	D20.5	101 10100	001011 1010	001011 1010
D5.4	100 00101	101001 1101	101001 0010	D21.5	101 10101	101010 1010	101010 1010
D6.4	100 00110	011001 1101	011001 0010	D22.5	101 10110	011010 1010	011010 1010
D7.4	100 00111	111000 1101	000111 0010	D23.5	101 10111	111010 1010	000101 1010
D8.4	100 01000	111001 0010	000110 1101	D24.5	101 11000	110011 1010	001100 1010
D9.4	100 01001	100101 1101	100101 0010	D25.5	101 11001	100110 1010	100110 1010
D10.4	100 01010	010101 1101	010101 0010	D26.5	101 11010	010110 1010	010110 1010
D11.4	100 01011	110100 1101	110100 0010	D27.5	101 11011	110110 1010	001001 1010
D12.4	100 01100	001101 1101	001101 0010	D28.5	101 11100	001110 1010	001110 1010
D13.4	100 01101	101100 1101	101100 0010	D29.5	101 11101	101110 1010	010001 1010
D14.4	100 01110	011100 1101	011100 0010	D30.5	101 11110	011110 1010	100001 1010
D15.4	100 01111	010111 0010	101000 1101	D31.5	101 11111	101011 1010	010100 1010

Table C1 (continued) - Valid Data Characters

Data Byte Name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj	Data Byte Name	Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table C1 (concluded) - Valid Data Characters

Special Code Name	Current RD - abcdei fghj	Current RD + abcdei fghj
K28.0	001111 0100	110000 1011
K28.1	001111 1001	110000 0110
K28.2	001111 0101	110000 1010
K28.3	001111 0011	110000 1100
K28.4	001111 0010	110000 1101
K28.5	001111 1010	110000 0101
K28.6	001111 1000	110000 1001
K23.7	111010 1000	000101 0111
K27.7	110110 1000	001001 0111
K29.7	101110 1000	010001 0111
K30.7	011110 1000	100001 0111

Table C2 - Valid Special Characters

The terminology of encoding used in table C1 is described as follows:

Data Byte	d7	d6	d5		d4	d3	d2	d1	d0	
8B Information Character	H	G	F		E	D	C	B	A	
10B Transmission Character	a	b	c	d	e	i		f	g	h	j

Bit a is transmitted first. Each transmission character in the table (Valid Data Character) is associated with a name Dx.y, where

x is the decimal value of the bits EDCBA

x*dec* = EDCBA*bin*

y is the decimal value of the bits HGF:

y*dec* = HGF*bin*

In addition there are further 10B code words named Valid Special Characters Kx.y, see table C2. Only the Special Character: K28.5 (Comma) is here used as stuffing data and for byte synchronization.

Example:

Encoding of the MPEG synchronous byte 47*hex* = 0100 0111.

8B Information Character	0	1	0		0	0	1	1	1		D7.2
10B Transmission Character	1	1	1	0	0	0		0	1	0	1	RD +
	0	0	0	1	1	1		0	1	0	1	RD -

Encoding depends on the parameter RD (Running Disparity). RD determines the ratio of zeros and ones during the transmission. Switching between the code words depending on the RD in the Transmitter and Receiver maintains the DC balance. RD is calculated based on two sub-blocks: bits abcdei and bits fghj of the Transmission Character. RD at the beginning of a sub-block is the calculated RD of the last sub-block. RD at the end of any sub-block is positive, if the sub-block contains more ones than zeros, or if the sub-block is 000111 or 0011. RD at the end of any sub-block is negative, if the sub-block contains more zeros than ones, or if the sub-block is 111000 or 1100. Otherwise the last RD is taken. Initialization of the transmitter is done with negative RD, the transmitter may assume either the positive or the negative RD. Independent of the validity of the transmission characters the received transmission characters shall be used as the receiver's current RD for the next transmission character.

The redundancy of the 8B/10B transmission code can be used for error detection.

Code violations may result from a prior error which altered the RD of the bit stream, causing a detectable error at the current transmission character. The example in table C3 shows this behavior.

Table C3 - Delayed Code Violation Example

	RD	Character 1	RD	Character 2	RD	Character 3	RD
Transmitted character stream	-	D21.1	-	D10.2	-	D23.5	+
Transmitted bit stream	-	101010 1001	-	010101 0101	-	111010 1010	+
Bit stream after error	-	101010 1011	+	010101 0101	+	111010 1010	+
Decoded character stream	-	D21.0	+	D10.2	+	Code violation	+

Annex D (informative): Implementation guidelines and clock recovery from the Synchronous Serial Interface (SSI)

D1 Example of implementation of the SSI interface

Hardware implementation of the proposed SSI interface was undertaken in order to validate the serial transmission in a real MPEG2 chain including TS multiplexer, QPSK mod/demod, QAM mod/ demod.

It consists of two adapter modules:

- an emitting module which transforms the parallel interface, such as described in 5.1 into the serial mode;

- a receiving module which performs the reverse function in recovering the transport packets conforming to the parallel interface.

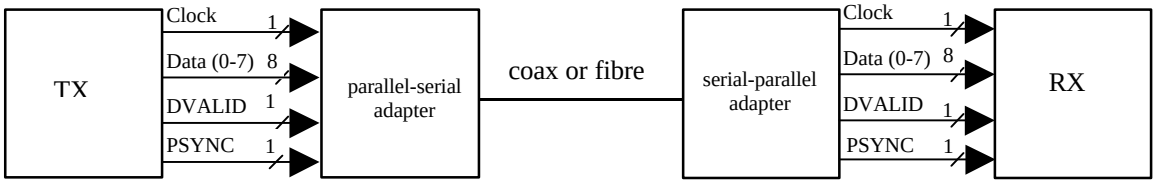


Figure D1 - Connection of the adapter modules

D1.1 Emitting module

The main functions are:

- The parallel to serial conversion,
  The generation of the serial clock by a multiplication by 8 of the parallel clock. As an example, the "programmable skew clock buffer" (CYPRESS-CY7B991) is well suited for that application.

- Biphase-Mark encoding .
  Example: the 50Mbit Manchester biphase-mark encoder (PLESSEY-SP9960)

- LED driver for optical transmission
  The PLESSEY-SP9960 has a built-in LED driver.

- Cable driver for coaxial transmission

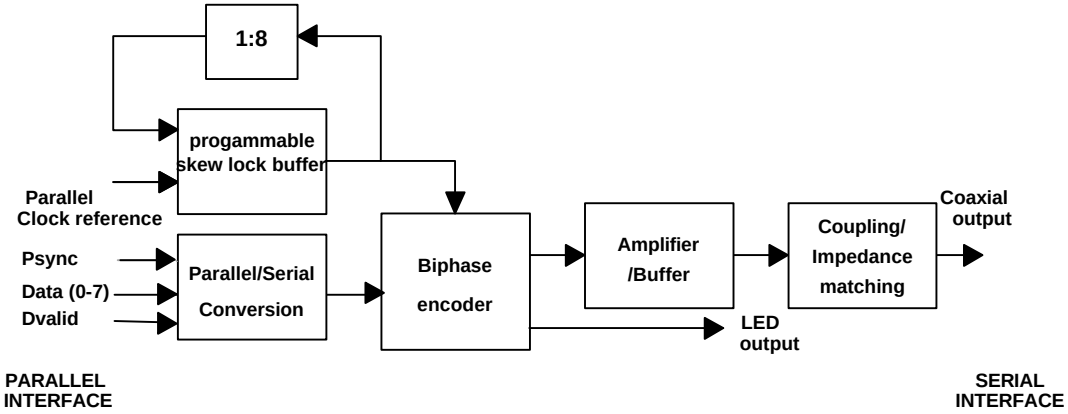


Figure D2 - Example of implementation of an emitting module

D1.2 Receiving module

The byte synchronization process in the receiving equipment has to take into account the two possible packet formats, i.e. the 188 byte-packet format and the 204-packet format.

An automatic byte synchronization was performed as follows:

- a first attempt of synchronization can be done on the hypothesis of 188 byte-packet format;
- if the first attempt is unsuccessful, the synchronization is done on the 204 byte-packet format.

The main functions are:

- Cable equalizer for coaxial reception

- Optical receiver for optical reception

- Clock recovering and Biphase-Mark decoding .
  As an example, the 50 Mb/s Manchester biphase decoder (PLESSEY-SP9921) operates from 20 Mbit/s to 50 Mbit/s

- Byte synchronization and deserialization

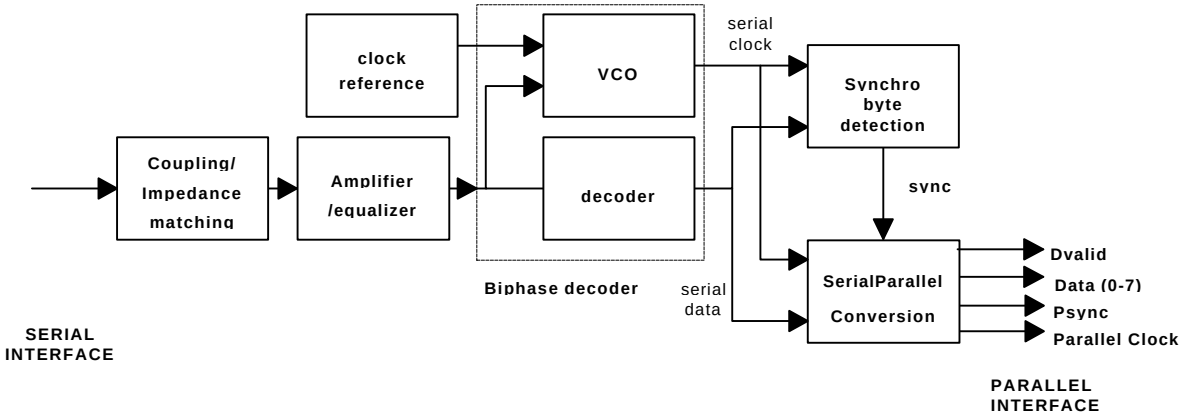


Figure D3 - Example of implementation of a receiving module

A receiving module capable of receiving a Transport Stream of any frequency within a certain predefined frequency range can be designed according to the following principle:

- A signal which indicates if the PLL is locked or not has to be present
- If the PLL is not locked, the value of the reference clock is changed step by step until the PLL is locked.

Using this approach with the PLESSEY-SP9921 biphase decoder, an automatic reception of any TS rates from 20 Mbit/s to 50 Mbit/s was achieved. This example covers a representative range of applications in broadcasting areas.

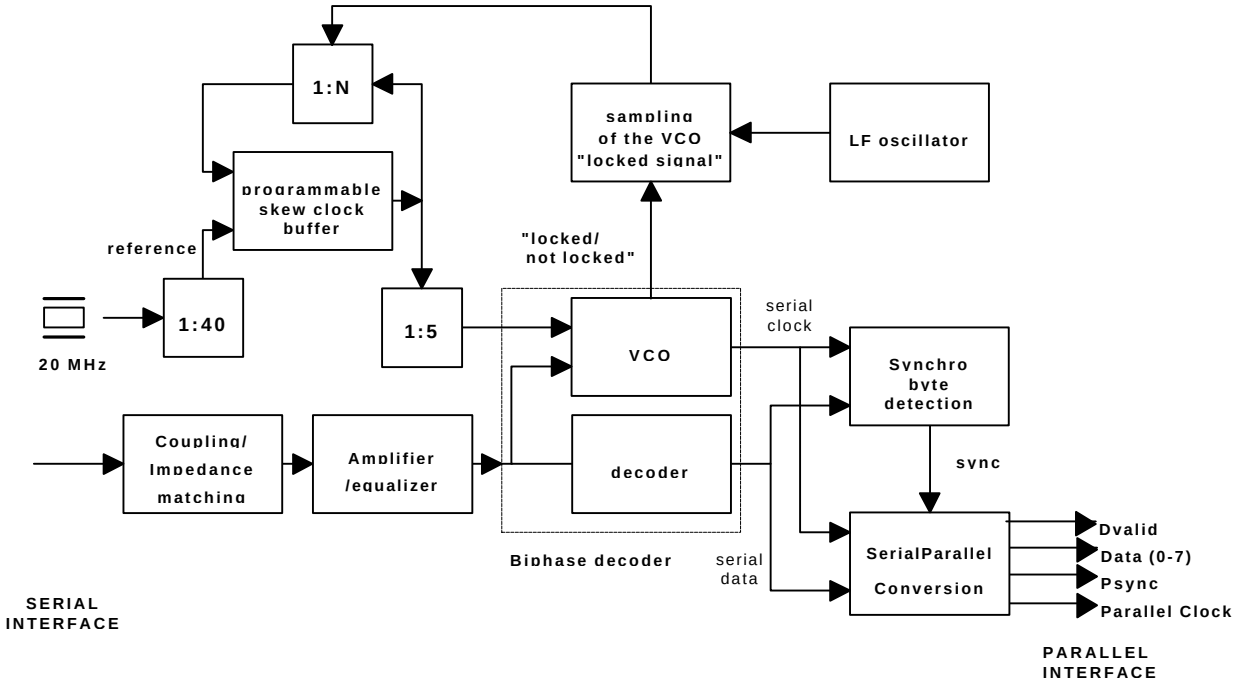


Figure D4 - Example of implementation of an automatic receiving module for SSI

D2 Physical Media

Different physical media can be used :

Coaxial cable:

Equalization of 12 dB at 70 MHz assuming a $1/\sqrt{f}$ attenuation law. As an example links of more than 100 m can be handled with KX 6 (equivalent to RG59 BU) coaxial cable and links of more than 200 m can be handled with KX 8 (equivalent to RG 216U) coaxial cable for a data rate up to 70 Mbit/s.

Optical Fibre:

Multimode or Singlemode: several km, depending on configuration.

Annex E (informative): Implementation guidelines and deriving clocks from the MPEG-2 Packets for the ASI

The ASI receiver generally is the input part of a complex device such as a modulator, a multiplexer or an adapter for telecommunications networks. The MPEG specification offers different possibilities for the regeneration of a valid MPEG transport stream.

Figure E1 shows two applications: the transport stream clock either is determined by the subsequent equipment or extracted from the transmitted signal itself.

Concerning clock generation from an ASI data stream, information on the PLL circuitry is given in the following.

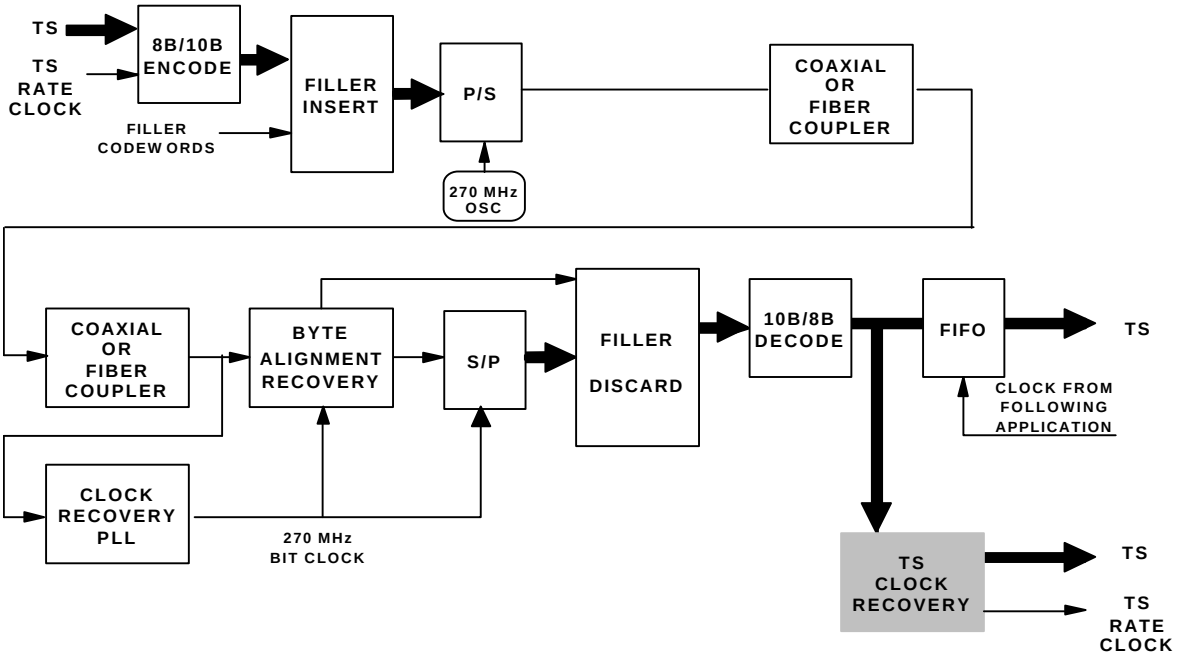


Figure E1 - ASI link with output clock from following application or alternative with clock recovery.

The induced jitter from the ASI itself is only about ±40ns. Consequently, there is little need for clock/rate recovery in most distribution systems. However, in those circumstances which may require transport rate recovery or smoothing, the following example illustrates the feasiblity of locking to the transport rate via the packet sync byte.

In order to ensure that the channel's delivery rate frequency lock loop is useful for both packets which are delivered in bursts and those which are linearly distributed, it is suggested that the loop use the packet sync byte for timing. For this example it is assumed that the MPEG-2 packets arrive at a nominal 10 kHz rate corresponding to a bit rate of 15,04 Mbit/s. By phase locking to the sync byte arrival, a packet clock and a bit clock can be derived. The circuit to be used is a second order phase-locked loop (PLL) as shown in figure E2. The sync

byte detector produces a time error between the detected and the hypothesized arrival times. This error drives a second order loop filter which in turn controls a VCO or a PLL that operates near the 10 kHz rate. This clock can be multiplied up by 1504 to generate a bit rate clock.

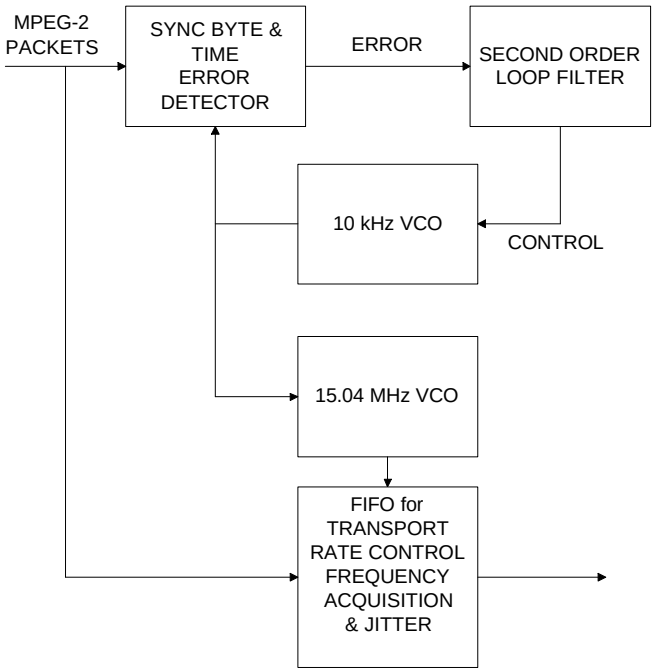


Figure E2 - Phase-Locked Loop for Clock Generation

It is also assumed in this simplified example that the transport rate must be known in order to set the loop multiplier due to the wide range of rates which must be tracked. Of course, MPEG clock timing constraints are also assumed.

A FIFO buffer is included in this example in order to

* provide a smoothing buffer for the output rate control mechanism;
* provide a clock acquisition buffer to account for the initial rate differential between input and output as the PLL adapts to the changing transport rates with possibly different (up to 60ppm) rate clocks;
* buffer the packet jitter which may be introduced by the interface or attached equipment (likely to be very small).

Table E1 contains a Mathcad 5.0 analysis and simulation of the difference equations comprising a digital implementation of the circuit in figure E2.

The assumptions are that the arrival rate is 10 kHz with a ±50 μsec uniform jitter (θ_n). The loop constants *K1* and *K2* are chosen to make the damping factor 0,707 and the loop bandwidth 52,5 Hz, assuming a 10 kHz sample rate. The variable $ACCT_n$ is the accumulator in the loop filter, and it converges to the time interval between arriving sync bytes. Consequently, its inverse is the rate at which sync bytes arrive. The first curve shows this rate converging to 10 kHz after about 700 samples (0,07 sec). The frequency accuracy is shown by computing the mean *(Amean*) and standard deviation (*Asd*) of this inverse. The next set of calculations show the clock accuracy in seconds with the standard deviation being about 19 nsec. The deviation, or jitter, may be traded for acquisition time, as an MPEG-2 decoder will certainly accept more than19 nsec of apparent packet jitter.

Table E2 shows a Mathcad analysis and simulation for the circuit of figure E2 operating with a delivery rate that jitters at ±2 msec. Note that the loop still acquires synchronisation in about 700 samples, or 0,07sec. The accuracy of the derived clock is depicted by *Amean* and *Asd* for the frequency, and *Tmean* and *Tsd* for the time. The standard deviation of the time is now 765 nsec, or about 40 times the results of table E1. This is still very small relative to the currently suggested real time jitter constraint for MPEG-2 decoders.

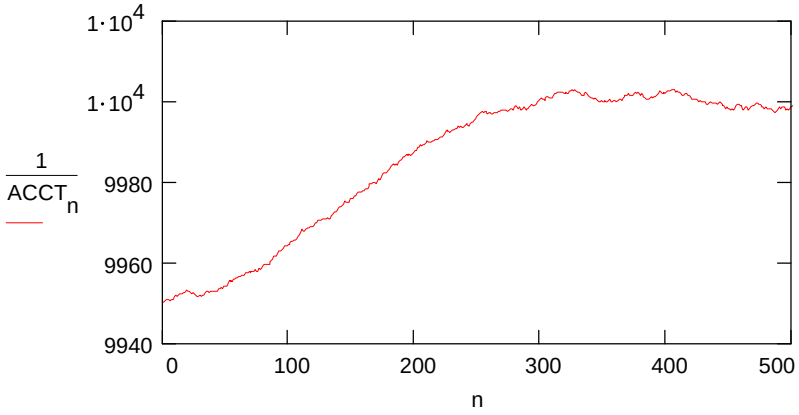
Table E1 - Analysis of 10 kHz Clock Generating Loop, ± 50µsec jitter

$n := 0..20000 \qquad K1 := .014 \qquad K2 := .000098$

$T_0 := .0001$

$$\begin{bmatrix} \phi_0 \\ ACCT_0 \\ ACCP_0 \end{bmatrix} := \begin{pmatrix} 0 \\ 1.005 \cdot T_0 \\ 0 \end{pmatrix} \qquad \theta_n := 1.0 \cdot (rnd(1) - .5)$$

$$\begin{bmatrix} \phi_{(n+1)} \\ ACCT_{(n+1)} \\ ACCP_{(n+1)} \end{bmatrix} := \begin{bmatrix} (n \cdot 1.00 + \theta_n) \cdot T_0 - ACCP_n \\ ACCT_n + K2 \cdot \phi_n \\ ACCP_n + K1 \cdot \phi_n + ACCT_n \end{bmatrix}$$



$$Amean := \frac{1}{10000} \cdot \left[\sum_{n=10001}^{20000} \left(\frac{1}{ACCT_n} \right) \right] \qquad Tmean := \frac{1}{10000} \cdot \sum_{n=10001}^{20000} ACCT_n$$

$Amean = 1.000005167 \cdot 10^4$ $\qquad$ $Tmean = 0.000099999487$

$$Asd := \sqrt{\frac{1}{10000} \cdot \sum_{n=10001}^{20000} \left(\frac{1}{ACCT_n} - Amean \right)^2} \qquad Tsd := \sqrt{\frac{1}{10000} \cdot \sum_{n=10001}^{20000} \left[\left(ACCT_n \right) - Tmean \right]^2}$$

$Asd = 1.9119$ $\qquad$ $Tsd = 1.9118 \cdot 10^{-8}$

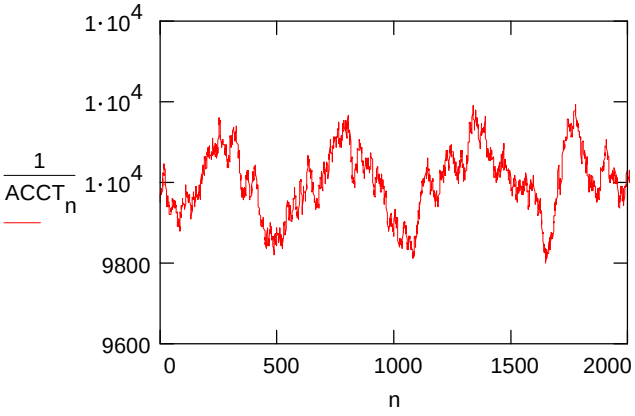
Table E2 - Analysis of 10 kHz Clock Generating Loop, ± 2 msec jitter

$n := 0..20000 \qquad K1 := .014 \qquad K2 := .000098$

$T_0 := .0001$

$$\begin{bmatrix} \phi_0 \\ ACCT_0 \\ ACCP_0 \end{bmatrix} := \begin{pmatrix} 0 \\ 1.005 \cdot T_0 \\ 0 \end{pmatrix} \qquad \theta_n := 40 \cdot (rnd(1) - .5)$$

$$\begin{bmatrix} \phi_{(n+1)} \\ ACCT_{(n+1)} \\ ACCP_{(n+1)} \end{bmatrix} := \begin{bmatrix} (n \cdot 1.00 + \theta_n) \cdot T_0 - ACCP_n \\ ACCT_n + K2 \cdot \phi_n \\ ACCP_n + K1 \cdot \phi_n + ACCT_n \end{bmatrix}$$



$$Amean := \frac{1}{10000} \cdot \left[\sum_{n=10001}^{20000} \left(\frac{1}{ACCT_n} \right) \right] \qquad Tmean := \frac{1}{10000} \cdot \sum_{n=10001}^{20000} ACCT_n$$

$Amean = 1.000263885 \cdot 10^4$ $\qquad$ $Tmean = 9.997947721 \cdot 10^{-5}$

$$Asd := \sqrt{\frac{1}{10000} \cdot \sum_{n=10001}^{20000} \left(\frac{1}{ACCT_n} - Amean \right)^2} \qquad Tsd := \sqrt{\frac{1}{10000} \cdot \sum_{n=10001}^{20000} \left[(ACCT_n) - Tmean \right]^2}$$

$Asd = 76.636$ $\qquad$ $Tsd = 7.647 \cdot 10^{-7}$

Annex F (informative):Bibliography

The following documents, although not normative documents, are related to this specification or contain useful additional information in relation to this specification.

ETS 300 421	Digital broadcasting for television, sound and data services; framing structure, channel coding and modulation for 11/12 GHz satellite services
ETS 300 429	Digital broadcasting for television, sound and data services; Framing structure, channel coding and modulation for Cable Systems